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Low-Voltage Differential Signaling (LVDS), Part 1

LVDS provides higher bit rates, lower power, and improved noise performance.

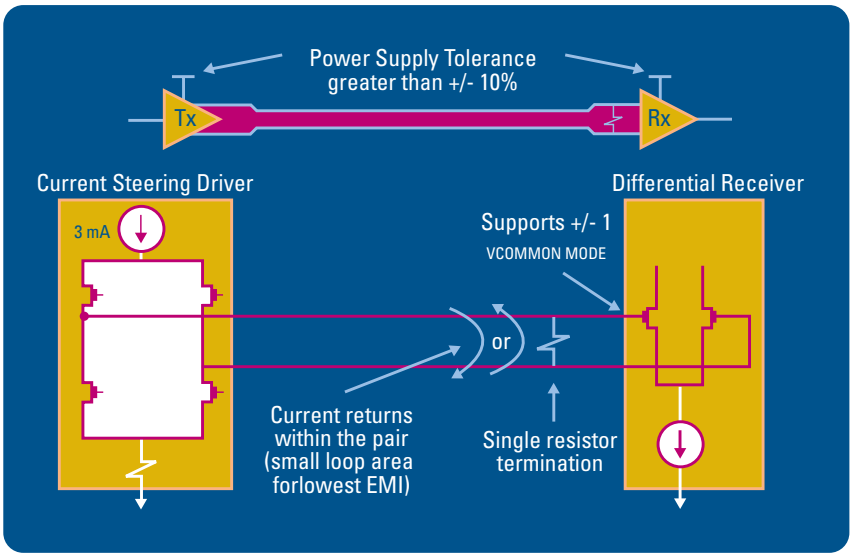


Figure 1. The equivalent circuit structure of the LVDS physical layer.

Due to the Internet's tremendous growth, data transfers are increasing dramatically in all areas of communications. In addition, data streams for digital video, HDTV, and color graphics are requiring higher and higher bandwidth. The digital communications deluge is the driving force for high-speed interconnects between chips, functional boards, and systems. The data may be digital, but it is analog Low-Voltage Differential Signaling (LVDS) that designers are choosing to drive these high-speed transmission lines. LVDS's proven speed, low power, noise control, and cost advantages are popular in point-to-point applications for telecommunications, data communications, and displays. LVDS uses high-speed analog circuit techniques to provide multi-gigabit data transfers on copper interconnects.

Wherever you need high-speed data transfer (100 Mb/s and higher), LVDS offers a solution. There are many applications in many market segments that use LVDS for data transmission. These include:

- stackable hubs for data communications
- wireless base stations and ATM switches in telecommunications
- flat-panel displays and servers in the computer market
- peripherals like printers and digital copy machines
- high-resolution displays in industrial applications
- flat-panel displays in the automotive market

In these applications, high-speed data moves within and between systems. Moving data within a system (intra-system data transfer) is the main use for LVDS solutions today. Moving information between systems (inter-system data transfer) requires standard communication protocols such as IEEE 1394, Fibre Channel, and Gigabit Ethernet. Since the hardware and software overhead for inter-system protocols is too expensive to use for intra-system data transfers, a simple and low-cost LVDS link is an attractive alternative. Thus, LVDS solutions move information on a board, between boards, modules, shelves, and racks, or box-to-box. The transmission media can be copper cables or printed circuit board (PCB) traces. In the future, LVDS will also carry protocols for inter-system communication.

Generic LVDS

Low-Voltage Differential Signaling is a generic interface standard for high-speed data transmission. The ANSI/TIA/EIA-644-1995 standard specifies the physical layer as an electronic interface. This standard defines driver and receiver electrical characteristics only. It does not define protocol, interconnect, or connector details because these details are application specific. The LVDS Standard's Working Group chose to define only the electrical characteristics to ensure that LVDS becomes a multi-purpose interface standard. Therefore, each application that uses LVDS should also reference the appropriate protocol and interconnect standard.

The equivalent circuit structure of the LVDS physical layer is shown in **Figure 1**. In the driver, a current source limits output to about 3 mA, and a switch box steers the current through the termination resistor. This differential driver produces odd-mode transmission: equal and opposite currents flowing in the transmission lines. The current returns within the wire pair, so the current loop area is small, and therefore generates the lowest amount of EMI. The current source limits any spike current that could occur during transitions. Because there are no spike currents, data rates as high as 1.5 Gb/s are possible without a substantial increase in power dissipation. In addition, the constant current driver output can tolerate transmission lines shorted together, or to Ground, without creating thermal problems.

The differential receiver is a high-impedance device that detects differential signals as low as 20 mV and then amplifies them into standard logic levels. The signal has a typical driver offset of 1.2 V, and the receiver accepts an input range of Ground to 2.4 V. This allows rejection of common-mode noise picked up along the interconnect of up to +/- 1 V.

In addition, hot plugging of LVDS drivers and receivers is possible because the constant current drive eliminates damage potential. Another feature is the receiver's failsafe function, which prevents output oscillations when the input pins are floating.

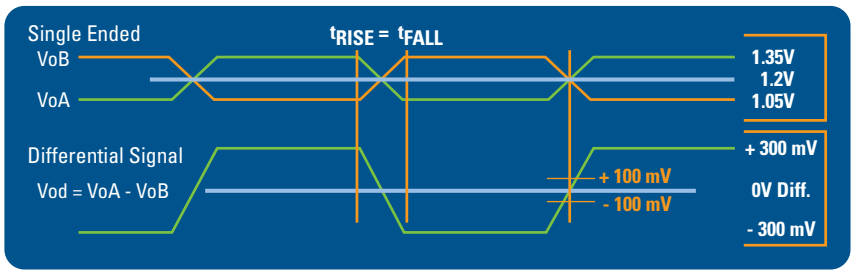
Multiple Technologies and Supply Voltages

When choosing the signal-level voltages for drivers and receivers, the standards committee considered LVDS implementation in technologies such as Bipolar, BiCMOS, CMOS, and even GaAs. In addition, the working group targeted a wide range of power supplies (such as 5 V, 3.3 V, and 2.5 V) for implementing LVDS, to ensure that LVDS would be the interface of choice for future generations of products.

Low-voltage signals have many advantages, including fast bit rates, lower power, and better noise performance. Design engineers have previously used full-swing CMOS and LVTTL Logic, but as bit rates increase, these solutions become unattractive. More recently, designers have turned to reduced-swing technologies such as SSTL and GTL to gain speed, save power, and reduce noise. LVDS increases these advantages by lowering voltage swings to about 300 mV. To increase noise immunity and noise margins even further, LVDS uses differential data transmission. Differential signals are immune to common-mode noise, the primary source of system noise. Because its voltage change between logic states is only 300 mV, LVDS can change states very fast. An LVDS signal also changes voltage levels without a fast slew rate. Slowing the transition rate decreases the radiated field strength. Slower transitions reduce the problem of reflections from transmission-path impedance discontinuities, decreasing emissions and crosstalk problems. Low voltage swing reduces power consumption because it lowers the voltage across the termination resistors and lowers the overall power dissipation.

The diagram in **Figure 2** emphasizes the advantage of a low voltage swing for higher performance. For example, when the signal level changes 300 mV in 333 ps, the slew rate is only 0.9 V/ns, which is less than the 1 V/ns benchmark slew rate commonly acceptable for minimizing signal distortion and crosstalk. If you use the old benchmark that the rise and fall times should be no more than two thirds of the bit width, then signals with 333-ps transitions can operate as high as 1 Gb/s with plenty of margin.

Figure 2. The lowered voltage swing maintains high speed without excessive slew rate.



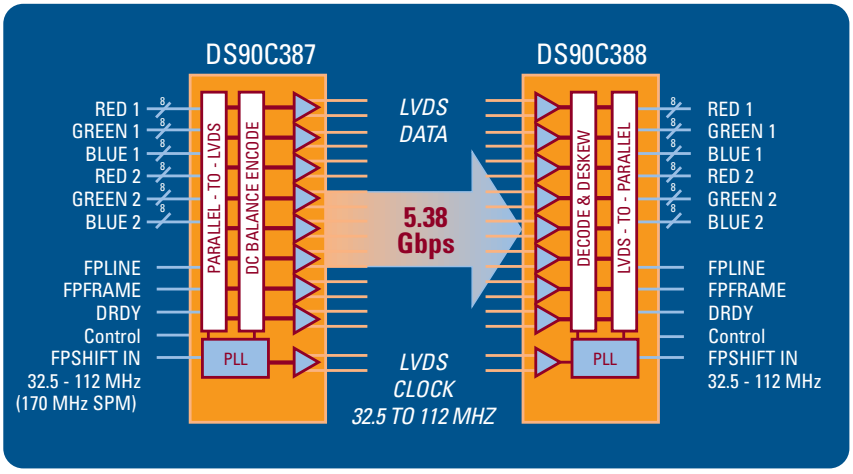


Figure 3. The OpenLDI (Open LVDS Display Interface) chipset is an example of LVDS's high performance.

Gigabits at Milliwatts

The simple phrase "Gigabits at milliwatts!" conveniently describes the benefits of an LVDS system. These benefits are high-speed data throughput, power-miser operation, noise control, low cost, and higher integration.

LVDS system features, such as serializing data, encoding the clock, and low skew, all work together for higher performance. Skew is a big problem for sending parallel data and its clock across cables or PCB traces. The problem is that the phase relation of the data and clock can be lost due to different travel times through the link. However, the ability to serialize parallel data into a high-speed signal with embedded clock eliminates the skew problem. The problem disappears because the clock travels with the data over the same differential pair of wires. The receiver uses clock and data recovery to extract the embedded clock, which is phase aligned to the data.

An example of LVDS's high performance is the OpenLDI (Open LVDS Display Interface) chipset that supports 24-bit color and provides throughput of over 5 Gb/s using only 8 data pairs and a clock pair **(Figure 3)**. The chipset serializes a 48-bit TTL interface down to the 8 pairs and then deserializes it at the receiver. The chipset supports TTL clock rates up to 112 MHz. To do this, each LVDS data channel serializes 6 TTL lines, plus a DC balance bit, into a single high-speed LVDS pair. That pair operates at 784 Mb/s with a data throughput of 672 Mb/s. The OpenLDI chipset can also operate at TTL bit rates as low as 33 Mb/s.

Besides giving tremendous throughput, the chipset reduces the interconnect width and provides other system benefits. The cable and connector are smaller and lower cost; the cable is more flexible, and the connector has fewer pins.

The beautiful eye pattern in **Figure 4** is taken at the end of a 5-meter cable between the Transmitter and Receiver of the OpenLDI chipset. The transmitter drives a Pseudo Random Bit Sequence through the cable, and the receiver recovers the signal. The markers show the bit width to be 1.275 ns, indicating a data rate of 784 Mb/s. Each of the 8 pairs carries this raw data rate, resulting in an aggregate bandwidth of almost 6.3 Gb/s. This data rate includes overhead for DC balance, so the actual payload bandwidth is 5.38 Gb/s.

Flat Supply Current vs. Operating Frequency

A significant advantage of LVDS technology is the lower power requirement. The graph in **Figure 5** shows LVDS's supply current remaining flat as the operating frequency increases, whereas the supply current for CMOS and GTL technology increases exponentially as frequency increases. LVDS benefits because it uses a constant-current line driver rather than a voltage-mode driver.

The load power calculation (3.3 mA times the 330-mV drop across the 100-Ω termination resistor) means LVDS has only 1.1-mW load power consumption. By comparison, GTL consumes 40 mA of load current through a 1-V drop across the load resistor, which is a whopping 40-mW load power dissipation. LVDS also has low power requirements compared to Pseudo ECL (PECL). The DS90C031 is an LVDS pin-compatible replacement part for the Pseudo ECL 41L Quad Differential Line Driver. The LVDS part consumes 16 times less supply current than the PECL part (3 mA compared to 50 mA). Furthermore, the low power consumption inherent in LVDS technology eliminates the need for either heat sinks or special packaging. This benefit also reduces the system cost of gigabit data transfers.

Another advantage of LVDS is its low electromagnetic-interference generation. The reasons LVDS generates low emissions are its low voltage swing, slow edge rates, the odd-mode differential signals, and the minimal I_{cc} spikes from constant current drivers. High-frequency signal transitions flowing through a transmission path create electromagnetic fields that radiate emissions. The field's strength is proportional to the energy carried by the signal. By reducing the voltage swing and the current energy, LVDS minimizes these fields. However, even the reduced electromagnetic fields can cause radiation problems.

Low Electromagnetic Interference

Differential signal paths reduce the harmful effects of these fields to further minimize these radiation problems. Balanced differential lines have equal but opposite currents, called odd-mode signals. When the fields created by these odd-mode signals are closely coupled, they tend to tie each other up and thus cannot escape to cause harm. Therefore, it is important to maintain a balanced and closely coupled differential transmission path to reduce emission of electromagnetic interference. Differential signals also have the advantage of tolerating interference from outside sources such as inductive radiation from electric motors or crosstalk from neighboring transmission lines. When the differential transmission lines are closely coupled, the induced signal is common-mode noise that appears as a common-mode voltage at the receiver input. The differential receiver responds only to the difference between the plus and the minus inputs, so when the noise appears commonly to both inputs, the input differential signal amplitude is undisturbed. This common-mode noise rejection also applies to noise sources such as power supply variations, substrate noise, and Ground bounce.

The LVDS Flat Panel Display (FPD) Link standard shown in **Figure 6** demonstrates the low noise-generation characteristics for LVDS while targeting LCD applications for notebook and sub-notebook computers. The FPD link moves large amounts of display data from the notebook PC to the display panel. The system designers had to solve the problem of twisted-pair cables or flex circuit carrying high-speed data through the panel hinge without creating EMI problems. They chose to use LVDS technology because it has better EMI performance than all other interface technologies.

Cost Benefits

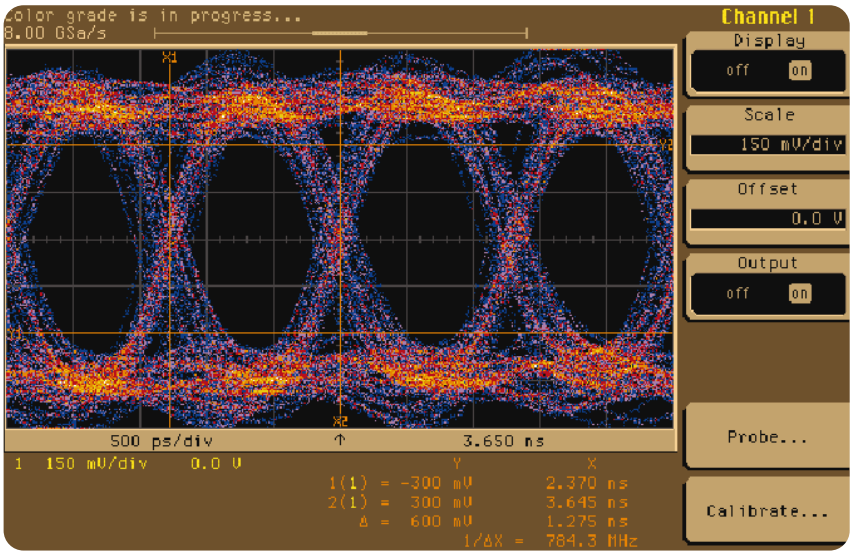
All of the LVDS advantages discussed so far also benefit system cost. There are even more system cost savings from using LVDS. The first is LVDS's ability to tolerate minor impedance mismatches in transmission paths. As long as the differential signal passes through balanced discontinuities in closely coupled transmission paths, the signal can maintain integrity. The effect of non-impedance-controlled connectors, printed circuit board vias, and chip packaging is not as detrimental to differential signals as it is to single-ended signals. In addition, it is possible to use fewer circuit board layers because of the relative immunity to crosstalk that is inherent in differential signals.

LVDS requires only a simple termination resistor, which can be integrated onto the chip. This costs much less than using multiple resistor and capacitor components for each transmission line. In addition, LVDS requires no termination or V_{ddq} voltage supply, a big cost savings over technologies such as GTL, LVTTL, and SSTL.

Because LVDS is capable of handling the high-speed data that results from serializing many parallel bits into a single data stream, LVDS chips commonly integrate serializers and deserializers. This saves about 50 percent of the cabling, connector, and PCB costs when compared to a parallel interconnect. The FPD-Link chipset demonstrates this system cost savings. The chipset takes the 18- or 24-bit-wide RGB (Red/Green/Blue) bus and the VSYNC, HSYNC, and Data Enable control lines and multiplexes them down to only 4 or 5 pairs. This low-cost 4- or 5-pair link passes data through the hinge to the panel where it is demultiplexed. Typical interconnects range from about 8 cm to 40 cm in length and use low-cost flex circuit or twisted-pair cabling.

The final LVDS system benefit is its integration capability. Because it is possible to implement high-speed LVDS in a standard CMOS process, integrating complex digital functions with LVDS's analog circuits is very beneficial. Integrating serializers and deserializers is only the beginning to mixed-signal LVDS chips.

Figure 4. Eye pattern measured at the end of a 5-meter cable between the Transmitter and Receiver of the OpenLDI chipset.



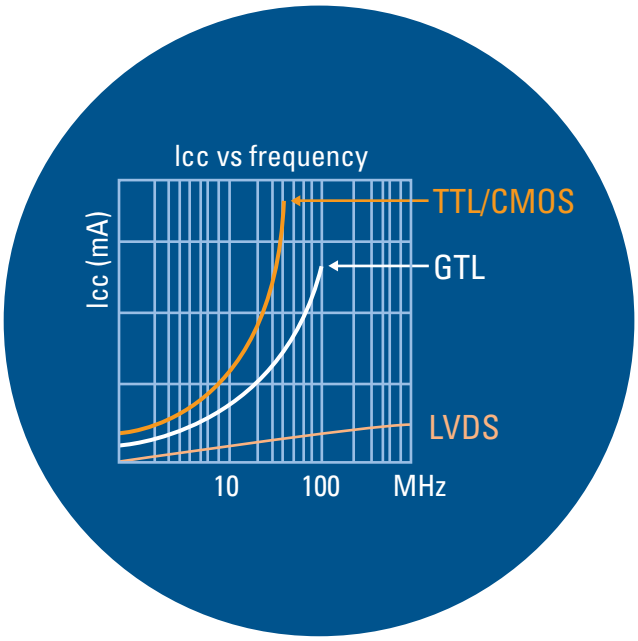


Figure 5. LVDS's supply current remains flat as the operating frequency increases.

Many Channels per Chip

LVDS's low power consumption enables integrating many channels per chip. For example, it is possible to serialize a 128-bit, on-chip parallel bus down to 8 differential channels. This narrower link dramatically reduces pin count and total link cost. Integration also benefits from differential signals. These signals tolerate high levels of switching noise, so they can be reliably integrated with large-scale digital circuits. In addition, LVDS generates very little noise due to the constant-current nature of the output structures. Therefore, complete interface Systems-on-a-Chip are feasible. Digital blocks for integration include DC Balance, Clock Embedding, Clock Recovery, Encoders and Decoders, and De-skew blocks. Higher-level digital functions such as hardware protocol assist, management and statistics counters, and routing decision logic are also using LVDS on-chip as the interface of choice. Further integration of the blocks shown in the FPD-Link chipset **(Figure 6)** is already happening. Obvious candidates for integration are the LVDS transmitter with the VGA controller and the LVDS receiver with the timing controller.

The OpenLDI chipset supports cable lengths up to 10 meters by integrating special functions. These functions are transmitter pre-emphasis, DC balance coding, and cable deskew. They all work to extend the reach and bandwidth of OpenLDI interconnects to flat-panel-monitor applications that may require longer cables.

DC Balance for Longer Cables

The OpenLDI chipset implements a simple DC balancing scheme that reduces inter-symbol interference (ISI). This demonstrates integrating digital functions onto the same chip as the LVDS interface. Without DC balance, a long cable can result in ISI for a single bit transition and cause a bit error. This happens because a single bit transition, after a long string of no transitions, may not contain the energy necessary to change the stored charge through the entire cable. The term "disparity" describes the stored charge on the cable. If the disparity magnitude is large, then the single bit transition cannot overcome the inter-symbol interference at the end of the cable.
The OpenLDI part provides DC balance on a frame-by-frame basis. During the frame, the transmitter monitors the input signal for transitions. If no transitions occur, the transmitter inverts the next frame to maintain balanced cable charge, thus keeping the disparity between plus 10 and minus 9. The 7th LVDS data bit indicates whether the data in the payload is "true" or "inverted".

This simple DC balance scheme keeps the signal eye diagram wide open at the receiver end. In addition, it provides enough DC balance to satisfy fiber-optical interconnect requirements, allowing the OpenLDI chipset to interface with standard parallel fiber-optical products.

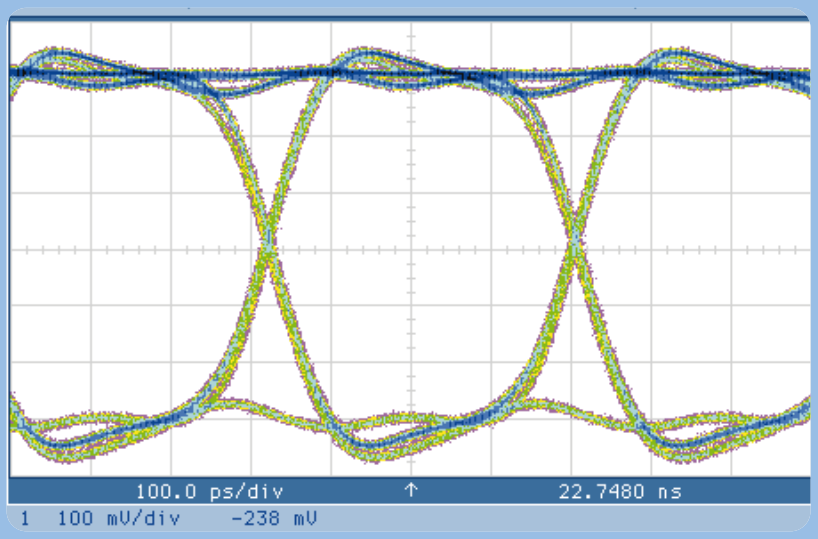
Figure 6. The LVDS Flat Panel Display Link moves large amounts of data from the notebook PC to the display panel.

Another integrated enhancement to the OpenLDI chipset is the transmitter pre-emphasis feature. Without pre-emphasis, the signal coming out of a cable loses the sharp transition edges due to the cable's high-frequency filter effect. With pre-emphasis, the driver accentuates the transitions to compensate for the filter effect at the end of the cable.

The pre-emphasis feature is user selectable. When pre-emphasis is selected, the transmitter has two current drive levels. It delivers additional dynamic current during transitions to overcome the cable's filtering, and supplies a lower drive current after the transition. It opens the signal eye diagram by overcoming cable distortion of the signal.

LVDS is now spawning follow-on technologies that expand its applications. The first follow-on is Bus LVDS, which allows the low-voltage differential signals to work in bi-directional and multi-drop configurations. Another LVDS derivative, Ground-referenced LVDS (GLVDS), is progressing through the standardization process. GLVDS moves the differential signal's common-mode voltage close to Ground, which allows chips operating from very low supply voltages to communicate over a high-speed standard interface. These "offspring" of LVDS will be the subject of part 2 of this article in the next issue of *Insight*.

See News & Events page 35 for information about our June 26 Web seminar that will address the ParBERT 81250.



ParBERT 81250 Simplifies the Characterization and Testing of LVDS Devices

The advantages of higher speed and better noise performance of LVDS devices must be thoroughly characterized before an LVDS device can be properly designed into a system. The Agilent Technologies ParBERT 81250 provides measurement capabilities that until now were difficult and time consuming to perform. The ParBERT 81250 is a modular instrument that provides parallel bit-error-ratio testing up to 2.66 Gb/s for up to 64 channels. It provides chip control signals, divided or multiplied clock signals, 1-Mb/s to 2.66-Gb/s operation with proprietary formats, as well as low-voltage differential signaling (LVDS) load generation or analysis. You can test SAN-related multiplexers and demultiplexers, including gigabit Ethernet, flat-panel-display links, Fibre Channel, and Infiniband. ParBERT 81250 is especially suitable for multiplexer and demultiplexer (mux/demux), or SERDES (serializer/deseralizer) testing used in telecommunications and system area network (SAN) ICs, multiple transmitter and receiver testing in manufacturing, and forward error correction (FEC) device testing.

Manufacturing test engineers responsible for testing multiple transmitters and receivers often find that reducing the cost per test is critical. The Agilent ParBERT 81250 and SpectralBER help by providing scalable VXI platforms that let designers customize the number of channels needed.

For designers who need to test SAN-related multiplexers or demultiplexers, including Gigabit Ethernet, flat-panel-display link, Fibre Channel, and Infiniband, the combination of the ParBERT 81250, 86130A BitAlyzer, and the 86100A Infiniium DCA helps solve physical high-speed design problems.

For more information, check 1 on the reply card, or visit http://www.agilent.com/find/insight6.